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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/656,596	09/05/2003	Wing K. Luk	YOR920030119US1	7956

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EXAMINER	
YOHA, CONNIE C	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/656,596	LUK ET AL.	
	Examiner	Art Unit	
	Connie C. Yoha	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-9,13, 15-21, 23* is/are rejected.

7)☐ Claim(s) *10-12,14 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *9/5/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

CONNIE C. YOHA
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 4/14/04 was considered.

2. Claims 1-23 are presented for examination.

Specification

3. The disclosure is objected to because of the following informalities:

Under the BRIEF DESCRIPTION OF THE DRAWINGS section, only a general description of figure 1, 5 and 6 are disclosed. A brief description for figure 1A, 1B, 1C, 5A, 5B, 6A, and 6B are required.

Claim Rejections - 35 USC э 112

4. Claims 4 and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

There is insufficient antecedent basis for the limitations.

In claim 4, recites the limitation of "wherein at least one of the secondary sense amplifiers".

In claim 13, recites the limitation of "wherein at lest two of the commands are executed".

Claim Rejections - 35 USC э 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1-2, 4-8, 9, 15-17, and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dietrich et al , Pat. No. 6351419 in view of Chen et al, Pat. No. 6108258.

With regard to claim 1, Dietrich discloses a DRAM (col. 1, line 14) (also with regard to claim 8 and 20), comprising: at least one primary sense amplifier (fig. 2, SSA1, SSA2), wherein the at least one primary sense amplifier has data storage and data write-back capability (col. 3, line 32-46) (col. 4, line 27-34) (also with regard to claim 5-7), and a single ended bitline structure, wherein a storage cell and the at least one primary sense amplifier are connected by a single bitline, wherein the DRAM has storage cells and bitlines (col. 5, line 10-13). Dietrich however does not disclose that the primary sense amplifier has at least two amplification stages. However, Chen discloses a sense amplifier device for use with a high-speed IC memory device having a first-stage and a second-stage circuits (fig. 2, 30 and 31), which in combination, constituted a positive feedback amplification loop coupled to the bit lines for amplifying the differential data signal on the bit lines to a detectable level. Therefore, it would have been obvious for one having an ordinary skill in the art at the time the invention was made to modify Dietrich's device to include a two amplification stages as taught by Chen's to allows the differential data signal on the bit lines to be quickly amplified to the

detectable level with a reduced sensing latency, thus increasing the access speed to the memory device. Also, even though the bit lines are increased in length, the sensing speed is not significantly affected. This feature can also help save circuit layout space (also with regard to claim 4 and 19).

With regard to claim 2, Dietrich discloses further a single ended global bitline structure (col. 5, line 5-13), wherein the at least one primary sense amplifier (fig. 2, SSA1, SSA2) and a second sense amplifier (fig. 2, SA) are connected by a single global bitline, wherein the DRAM has secondary sense amplifiers and global bitlines (col. 5, line 5-13).

With regard to claim 9 and 21, Dietrich discloses a DRAM, comprising: a single ended bitline structure, wherein the DRAM has bitlines (col. 5, line 5-13); a single ended global bitline structure, wherein the DRAM has global bitlines (col. 5, line 5-13); a plurality of primary sense amplifier (fig. 2, SSA1, SSA2) operationally engaging the bitlines and the global bitlines, wherein the primary sense amplifier have data storage and data write-back capability, and wherein the primary sense amplifiers are being capable to decoupled from the global bitlines (col. 3, line 32-46); an inherent full-wordline I/O structure, wherein essentially all memory cell that are simultaneously turned on by any one wordline are being operated on by associated sense amplifiers of the primary sense amplifiers, wherein the DRAM has memory cells and wordlines (col. 1, line 46-65); and a pipelined architecture (col. 1, line 22-24), wherein the DRAM is functioning in cycles and in each of the cycles an operation can be initiated, and wherein the pipelined architecture comprise synchronized operation of the single ended

bitlines structure, of the single ended global bitline structure, of the primary sense amplifiers, and of the full-wordline I/O structured (col. 3, line 61-col. 4, line 41) (col. 5, line 10-15) (also with regard to claim 15-17).

Claim Rejections - 35 USC э 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 3, 18 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dietrich et al , Pat. No. 6351419 in view of Chen et al, Pat. No. 6108258 and further in view of Issa, Pat. No. 6480424.

With regard to claim 3, 18 and 23, Dietrich and Chen, as applied in prior rejection, disclosed all claimed subject matter except the DRAM further comprises a small voltage swing design. However, Issa discloses a DRAM device having main and local sense amplifier using a limited voltage swing design to send the swing signal from the active local sense amplifier to the global sense amplifier (col. 6, line 28-29). Therefore, it would have been obvious for one having an ordinary skill in the art at the time the invention was made to incorporate the use of a small voltage swing design on the global sense amplifier to helps reduce power consumption and decrease access time (col. 7, line 53-59).

Allowable Subject Matter

7. Claim 10-12, 14 and 22 are objected as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Claim 13 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and rewritten in independent form to include all of the limitations of the base claim and any intervening claims.

The prior art of record does not show the limitation of a DRAM having in combination with other features, a reduced address space, wherein the reduced address space has no column address; wherein a Read command and a subsequent WriteBack commanded of the commands are executed in differing or in a single cycles.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure. Sugibayashi (6246622) and Sugibayashi (6075735) disclose a memory device having main and local sense amplifier.

10. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

11. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (571) 272-1799. The examiner can normally be reached on Mon. - Fri. from 8:00 A.M. to 5:30 PM. The examiner's supervisor, Hoai Ho, can be reached at (571) 272-1777. The fax phone number for this Group is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-0956.

13. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov Should you have questions on access to the Private Pair system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C. Yoha

March 2005

CONNIE C. YOHA
PRIMARY EXAMINER